REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY MM DD 03-03-20	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 3.3 V DUAL UNIVERSAL ASYNCHRONOUS RECEIVER / TRANSMITTER WITH 64 BYTE FIFO, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/03626**
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AMSC N/A

5962-V026-03

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 3.3 V dual universal asynchronous receiver / transmitter with 64-byte FIFO microcircuit, with an operating temperature range of -40°C to +110°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03626	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TL16C752B-EP	3.3 V dual universal asynchronous receiver / transmitter with 64-byte FIFO

1.2.2 Case outline(s). The case outlines shall be as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-026	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 3.6 V
Input voltage range (V_I)	-0.5 V to V_{CC} + 0.5 V
Output voltage range (V_O)	-0.5 V to V_{CC} + 0.5 V
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC})	2.7 V to 3.6 V
Input voltage range (V_I)	0 V to V_{CC}
High level input voltage (V_{IH})	0.7 V_{CC} to V_{CC} 3/
Low level input voltage (V_{IL})	0.3 V_{CC} 3/
Output voltage (V_O)	0 V to V_{CC} 4/
High level output current (V_{OH}) :	
with I_{OH} = -8 mA	V_{CC} – 0.8 V minimum 5/
with I_{OH} = -4 mA	V_{CC} – 0.8 V minimum 6/
Low level output current (V_{OL}) :	
with I_{OH} = -8 mA	0.5 V maximum 5/
with I_{OH} = 4 mA	0.5 V maximum 6/
Input capacitance (C_I)	18 pF maximum
Virtual junction temperature range (T_J)	+25°C to +125°C 7/
Oscillator / clock speed	48 MHz 8/
Clock duty cycle	50 % nominal
Supply current (I_{CC}) : 9/	
with 36 MHz, 3.6 V	20 mA nominal
with 5 MHz, 3.6 V	6 mA nominal
with sleep mode, 3.6 V	1.2 mA nominal
Operating free-air temperature range (T_A)	-40°C to +110°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “ recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

3/ Meets TTL levels, V_{IO}(min) = 2 V and V_{IH}(max) = 0.8 V on nonhysteresis inputs.

4/ Applies for external output buffers.

5/ These parameters apply for D7 D0.

6/ These parameters apply for $\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$, $\overline{\text{INIA}}$, INTB, $\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$, $\overline{\text{RXRDYA}}$, $\overline{\text{RXRDYB}}$, $\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$, TXA, TXB.

7/ These junction temperatures reflect simulated condition. Absolute maximum junction temperature is +150°C. The customer is responsible for verifying junction temperature.

8/ The internal oscillator cell can only support up to 24 MHz clock frequency to make the crystal oscillating when crystal is used. If external oscillator or other on board clock source is used, the device can work for input clock frequency up to 48 MHz.

9/ Measurement condition:

a) Normal operation other than sleep mode: V_{CC} = 3.3 V, T_A = 25°C. Full duplex serial activity on all serial (UART) channels at the clock frequency specified in the recommended operating conditions with divisor of one.

b) Sleep mode: V_{CC} = 3.3 V, T_A = 25°C. After enabling the sleep mode for all four channels, all serial and host activity is kept idle.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
$\overline{IOR}$ delay from chip select	t_{d1}		-40°C to +110°C	01	0		ns
Read cycle delay	t_{d2}				2 input clock periods		ns
Delay from $\overline{IOR}$ to data	t_{d3}					28.5	ns
Data disable time	t_{d4}					15	ns
$\overline{IOW}$ delay from chip select	t_{d5}				10		ns
Write cycle delay	t_{d6}				2 input clock periods		ns
Delay from $\overline{IOW}$ to output	t_{d7}	100 pF load				50	ns
Delay to set interrupt from MODEM input	t_{d8}	100 pF load				70	ns
Delay to reset interrupt from $\overline{IOR}$	t_{d9}	100 pF load				70	ns
Delay from stop to set interrupt	t_{d10}					1RCLK	Baud rate
Delay from $\overline{IOR}$ to reset interrupt	t_{d11}	100 pF load				70	ns
Delay from stop to interrupt	t_{d12}					100	ns
Delay from initial INT reset to transmit start	t_{d13}				8	24	Baud rate
Delay from $\overline{IOW}$ to reset interrupt	t_{d14}					70	ns
Delay from stop to set $\overline{RXRDY}$	t_{d15}					1	Clock

See footnote at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Delay from $\overline{IOR}$ to reset $\overline{RXRDY}$	t_{d16}		-40°C to +110°C	01		1	µs
Delay from $\overline{IOW}$ to set $\overline{TXRDY}$	t_{d17}					70	ns
Delay from start to reset $\overline{TXRDY}$	t_{d18}					16	Baud rate
Delay between successive assertion of $\overline{IOW}$ and $\overline{IOR}$	t_{d19}					4 input clock periods	Baud rate
Chip select hold time from $\overline{IOR}$	t_{h1}				0		ns
Chip select hold time from $\overline{IOW}$	t_{h2}				0		ns
Data hold time	t_{h3}				15		ns
Address hold time	t_{h4}				0		ns
Hold time from XTAL1 clock ↓ $\overline{IOW}$ or $\overline{IOR}$ release	t_{h5}				20		ns
Clock cycle period	t_{p1}, t_{p2}				20		ns
Oscillator / clock speed	t_{p3}	V_{CC} = 3 V				48	MHz
Reset pulse width	$t_{(RESET)}$				200		ns
Address setup time	t_{su1}				0		ns
Data setup time	t_{su2}				16		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Setup time from $\overline{IOW}$ or $\overline{IOR}$ assertion to XTAL1 clock ↑	t_{su3}		-40°C to +110°C	01	20		ns
$\overline{IOR}$ strobe width	t_{w1}				2 input clock period		ns
$\overline{IOR}$ strobe width	t_{w2}				2 input clock period		ns

1/ V_{CC} = 3.3 V ±10 % unless otherwise specified.

Case X

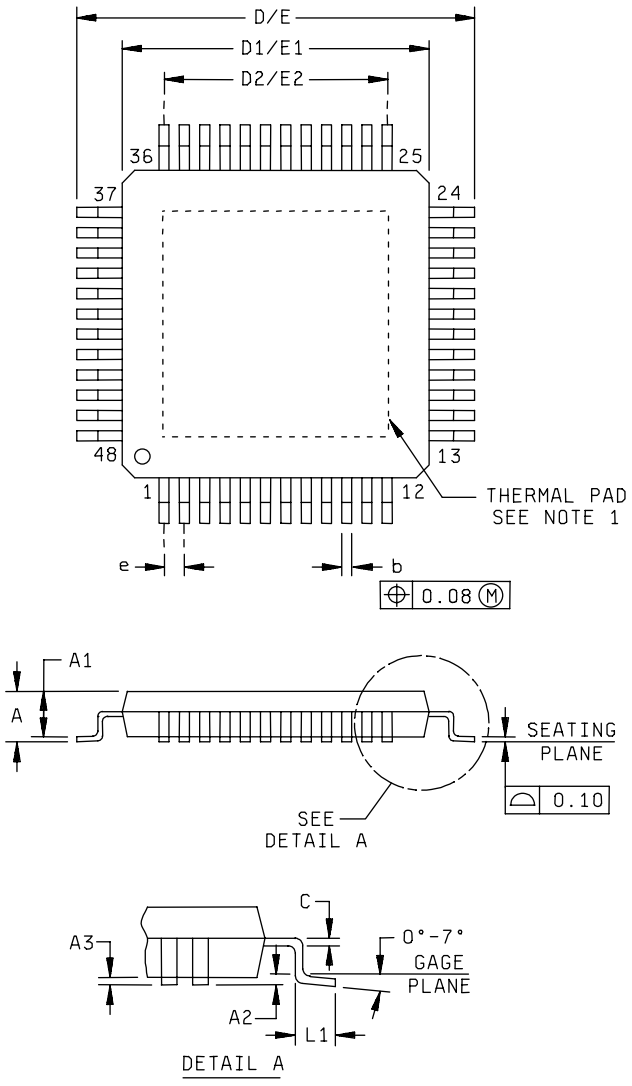

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03626
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Case X

Symbol	Dimensions	
	Millimeters	
	Min	Max
A		1.60
A1	1.35	1.45
A2	0.25	---
A3	0.05	---
b	0.17	0.27
C	0.13 nominal	
D	8.80	9.20
D1	6.80	7.20
D2	5.50 typical	
E	8.80	9.20
E1	6.80	7.20
E2	5.50 typical	
e	0.50	---
L1	0.45	0.75

NOTES:
1. The package thermal performance may be enhanced by bonding the thermal pad to an thermal plate. This pad is electrically and thermally connected to the backside of the die and possible selected leads.
2. Body dimensions do not include mold flash or protrusion.

FIGURE 1. Case outline – Continued.

Device types	All		Device types	All
Case outline	X		Case outline	X
Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	D5		25	NC
2	D6		26	A2
3	D7		27	A1
4	RXB		28	A0
5	RXA		29	INTB
6	$\overline{\text{TXRDYB}}$		30	INTA
7	TXA		31	$\overline{\text{RXRDYA}}$
8	TXB		32	$\overline{\text{OPA}}$
9	$\overline{\text{OPB}}$		33	$\overline{\text{RTSA}}$
10	$\overline{\text{CSA}}$		34	$\overline{\text{DTRA}}$
11	$\overline{\text{CSB}}$		35	$\overline{\text{DTRB}}$
12	NC		36	RESET
13	XTAL1		37	NC
14	XTAL2		38	$\overline{\text{CTSA}}$
15	$\overline{\text{IOW}}$		39	$\overline{\text{DSRA}}$
16	$\overline{\text{CDB}}$		40	$\overline{\text{CDA}}$
17	GND		41	$\overline{\text{RIA}}$
18	$\overline{\text{RXRDYB}}$		42	V_{CC}
19	$\overline{\text{IOR}}$		43	$\overline{\text{TXRDYA}}$
20	$\overline{\text{DSRB}}$		44	D0
21	$\overline{\text{RIB}}$		45	D1
22	$\overline{\text{RTSB}}$		46	D2
23	$\overline{\text{CTSB}}$		47	D3
24	NC		48	D4

NC = No internal connection

FIGURE 2. Terminal connections.

Terminal	I/O	Description
A0	I	Address 0 select bit. Internal registers address selection.
A1	I	Address 1 select bit. Internal registers address selection.
A2	I	Address 2 select bit. Internal registers address selection.
$\overline{CDA}$, $\overline{CDB}$	I	Carrier detect (active low). These inputs are associated with individual UART channels A and B. A low on these pins indicates that a carrier has been detected by the modem for that channel. The state of these inputs is reflected in the modem status register (MSR).
$\overline{CSA}$, $\overline{CSB}$	I	Chip select A and B (active low). These pins enable data transfers between the user CPU and the device for the channel(s) addressed. Individual UART sections (A, B) are addressed by providing a low on the respective $\overline{CSA}$ and $\overline{CSB}$ pins.
$\overline{CTSA}$, $\overline{CTSB}$	I	Clear to send (active low). These inputs are associated with individual UART channels A and B. A logic low on the CTS pins indicates the modem or data set is ready to accept transmit data from the device. Status can be tested by reading MSR bit 4. These pins only affect the transmit and receive operations when auto CTS function is enabled through the enhanced feature register (EFR) bit 7, for hardware flow control operation.
D0 – D7	I/O	Data bus (bidirectional). These pins are the eight bit, 3-state data bus for transferring information to or from the controlling CPU. Do is the least significant bit and the first data bit in a transmit or receive serial data stream.
$\overline{DSRA}$, $\overline{DSRB}$	I	Data set ready (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem or data set is powered on and is ready for data exchange with UART. The state of these inputs is reflected in the modem status register (MSR).
$\overline{DTRA}$, $\overline{DTRB}$	O	Data terminal ready (active low). These outputs are associated with individual UART channels A and B. A logic low on these pins indicates that the device is powered on and ready. These pins can be controlled through the modem control register. Writing a 1 to MCR bit 0 sets the $\overline{DTR}$ output to low, enabling the modem. The output of these pins is high after writing a 0 to MCR bit 0, or after a reset.
GND	Pwr	Signal and power ground.
INTA, INTB	O	Interrupt A and B (active high). These pins provide individual channel interrupts, INT A and B. INT A and B are enabled when MCR bit 3 is set to a logic 1, interrupt sources are enabled in the interrupt enable register (IER). Interrupt conditions include: receiver errors, available receiver buffer data, available transmit buffer space or when a modem states flag is detected. INTA-B are in the high-impedance state after reset.

FIGURE 2. Terminal connections – continued.

Terminal	I/O	Description
$\overline{IOR}$	I	Read input (active low strobe). A high to low transition on $\overline{IOR}$ loads the contents of an internal register defined by address bits A0-A2 onto the device data bus (D0-D7) for access by an external CPU.
$\overline{IOW}$	I	Write input (active low strobe). A low to high transition on $\overline{IOW}$ transfers the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined be address bits A0-A2 and $\overline{CSA}$ and $\overline{CSB}$.
$\overline{OPA}$, $\overline{OPB}$	O	User defined outputs. This function is associated with individual channels A and B. The state of these pins is defined by the user through the software settings of the MCR register, bit 3. INTA-B are set to active mode and $\overline{OP}$ to a logic 0 when the MCR-3 is set to logic 1. INTA-B are set to the 3-state mode and $\overline{OP}$ to a logic 1 when the MCR-3 is set to a logic 0. See bit 3, modem control register (MCR bit 3). The output of these two pins is high after reset.
RESET	I	Reset. RESET resets the internal registers and all the outputs. The UART transmitter output and the receiver input is disabled during reset time. See device external reset conditions for initialization details. RESET is an active high input.
$\overline{RIA}$, $\overline{RIB}$	I	Ring indicator (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem has received a ringing signal from the telephone line. A low to high transition on these input pins generates a modem status interrupt, if enabled. The state of these inputs is reflected in the modem status register (MSR).
$\overline{RTSA}$, $\overline{RTSB}$	O	Request to send (active low). These outputs are associated with individual UART channels A and B. A low on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a 1 in the modem control register (MCR bit 1) sets these pins to low, indicating data is available. After a reset, these pins are set to high. These pins only affect the transmit and receive operation when auto $\overline{RTS}$ function is enabled through the enhanced feature register (EFR) bit 6, for hardware flow control operation.
RXA, RXB	I	Receive data input. These inputs are associated with individual serial channel data to the device. During the local loop back mode, these RX input pins are disabled and TX data is internally connected to the UART RX input internally.
$\overline{RXRDYA}$, $\overline{RXRDYB}$	O	Receive ready (active low). $\overline{RXRDY}$ A and B goes low when the trigger level has been reached or a timeout interrupt occurs. They go high when the RX FIFO is empty or there is an error in RX FIFO.

FIGURE 2. Terminal connections – continued.

Terminal	I/O	Description
TXA, TXB	O	Transmit data. These outputs are associated with individual serial transmit channel data from the device. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX input.
$\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$	O	Transmit ready (active low). $\overline{\text{TXRDY}}$ A and B go low when there are at least a trigger level number of spaces available. They go high when the TX buffer is full.
V_{CC}	I	Power supply inputs.
XTAL 1	I	Crystal or external clock input. XTAL 1 functions as a crystal input or as an external clock input. A crystal can be connected between XTAL 1 and XTAL 2 to form an internal oscillator circuit. Alternatively, an external clock can be connected to XTAL 1 to provide custom data rates.
XTAL 2	O	Output of the crystal oscillator or buffered clock. See also XTAL 1. XTAL 2 is used as a crystal oscillator output or buffered a clock output.

FIGURE 2. Terminal connections – continued.

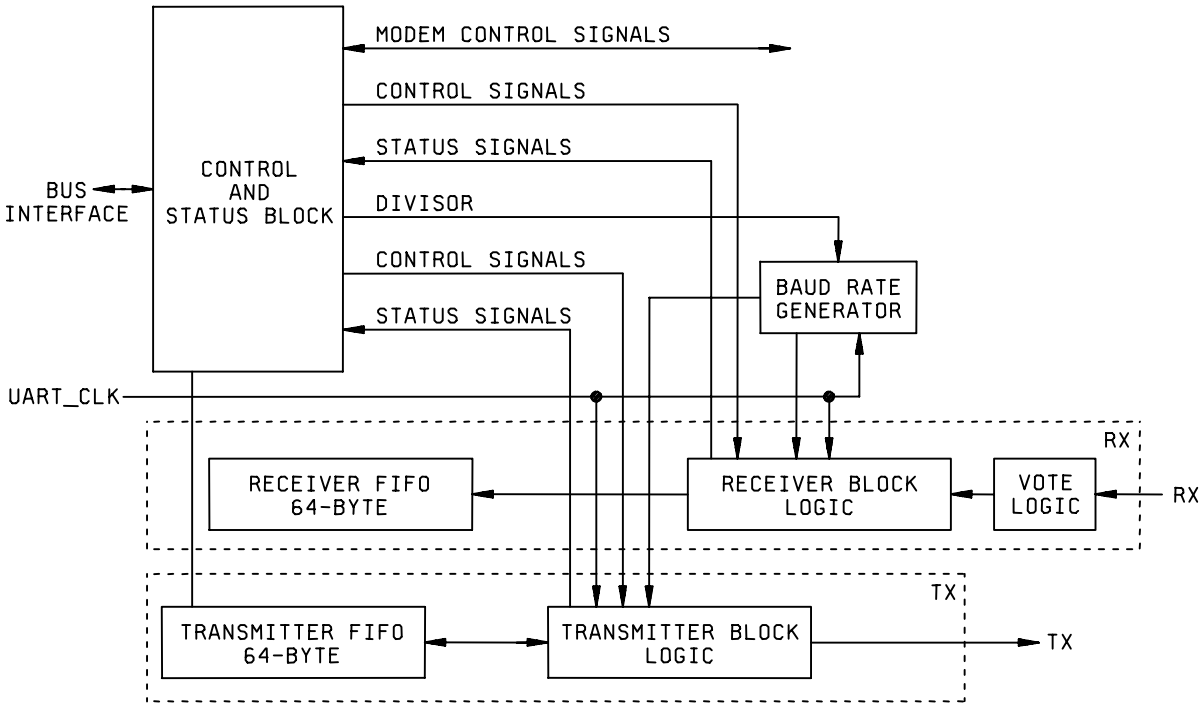
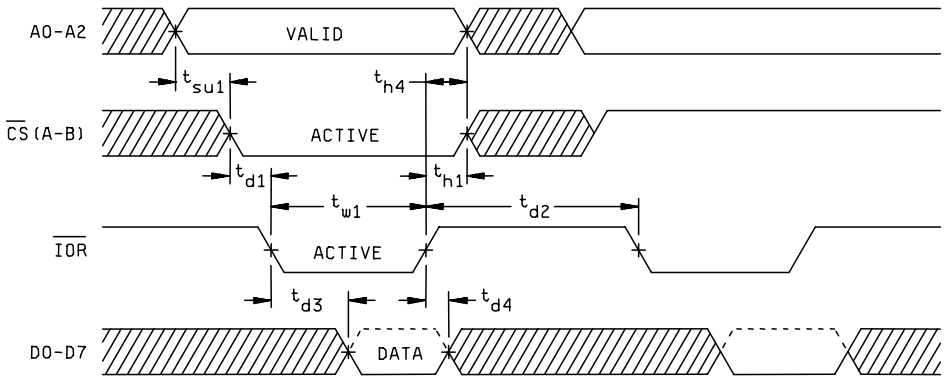
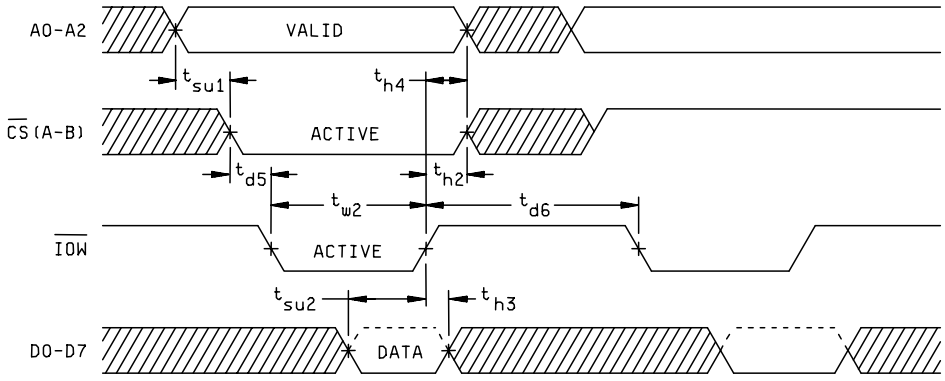


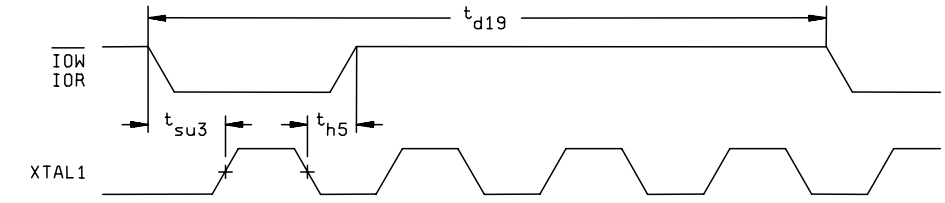
FIGURE 3. Block diagram.



GENERAL READ TIMING



GENERAL WRITE TIMING



ALTERNATE READ/WRITE STROBE TIMING

FIGURE 4. Timing waveforms.

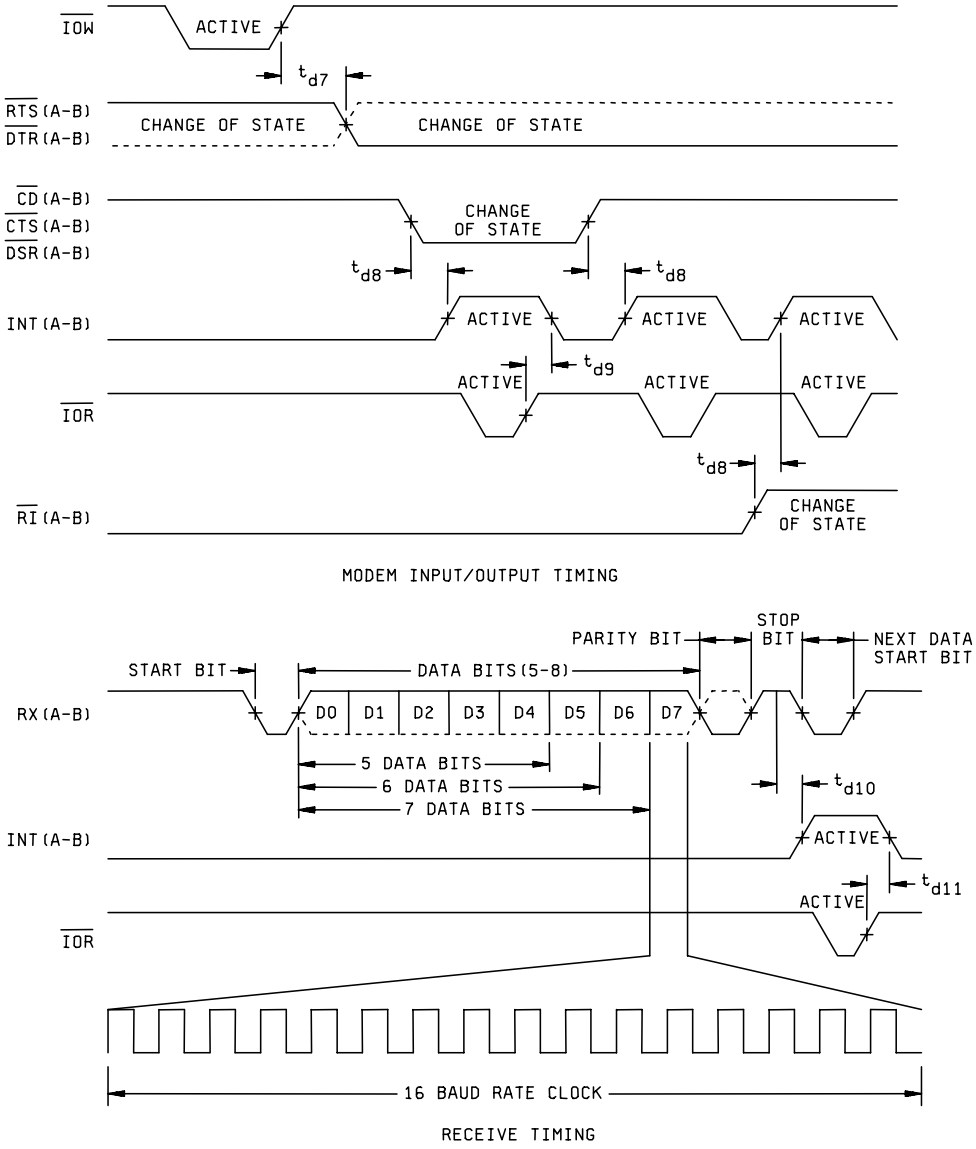
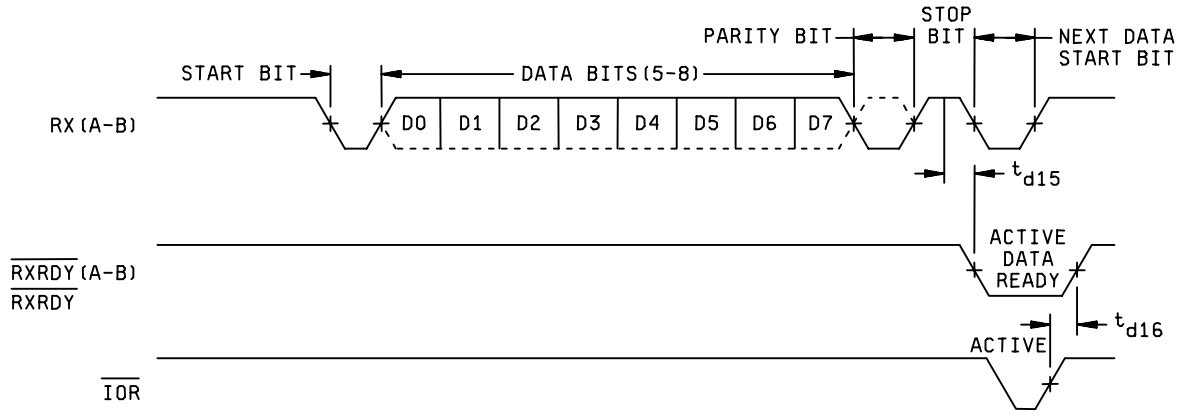
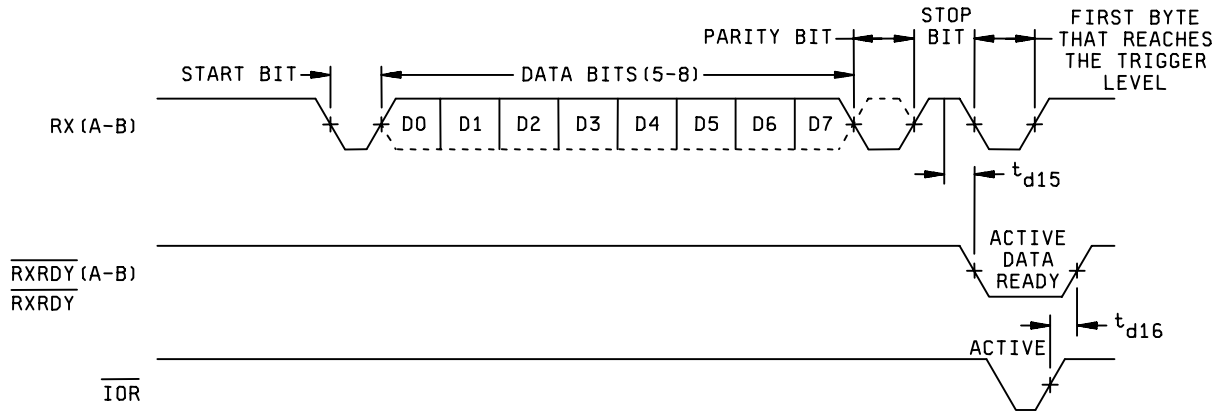


FIGURE 4. Timing waveforms – continued.

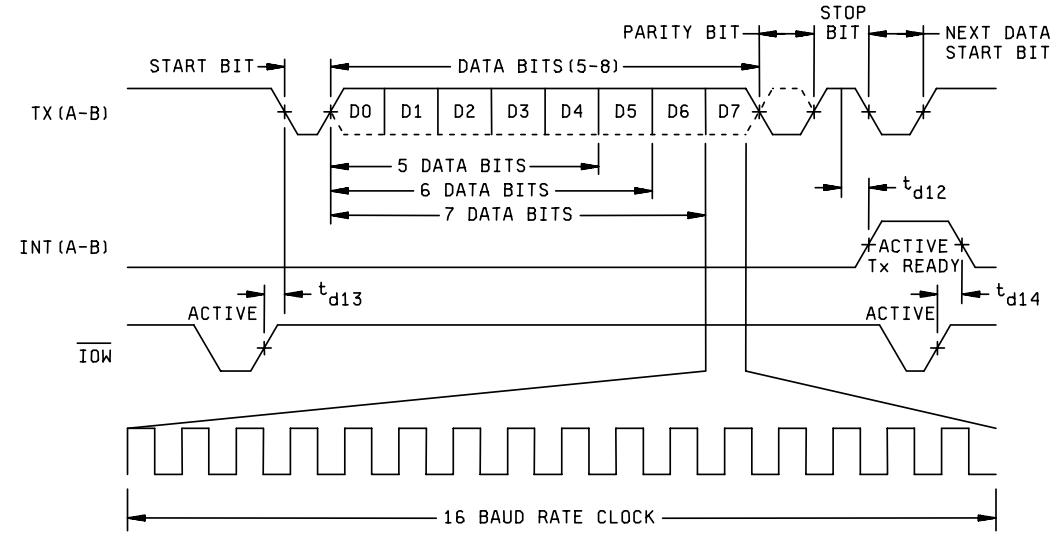


RECEIVE READY TIMING IN NON-FIFO MODE

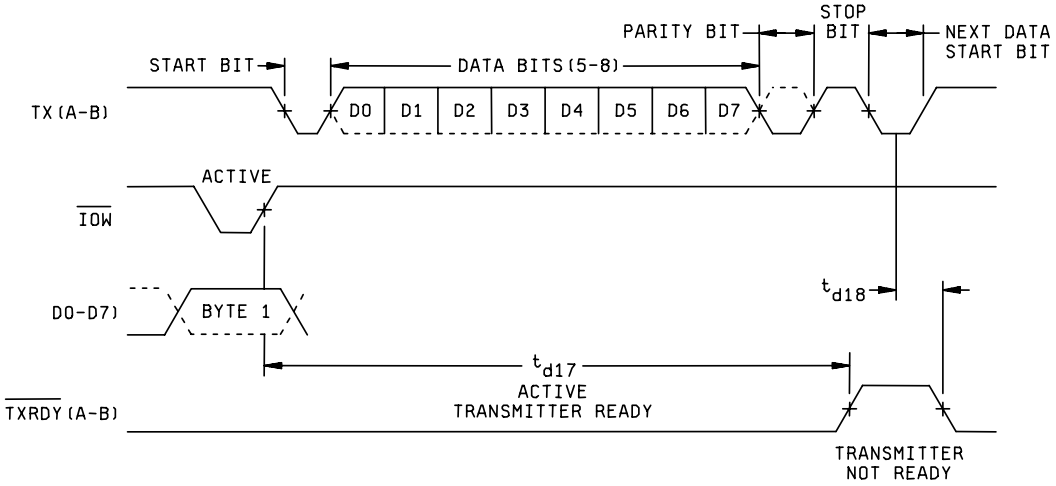


RECEIVE READY TIMING IN FIFO MODE

FIGURE 4. Timing waveforms – continued.

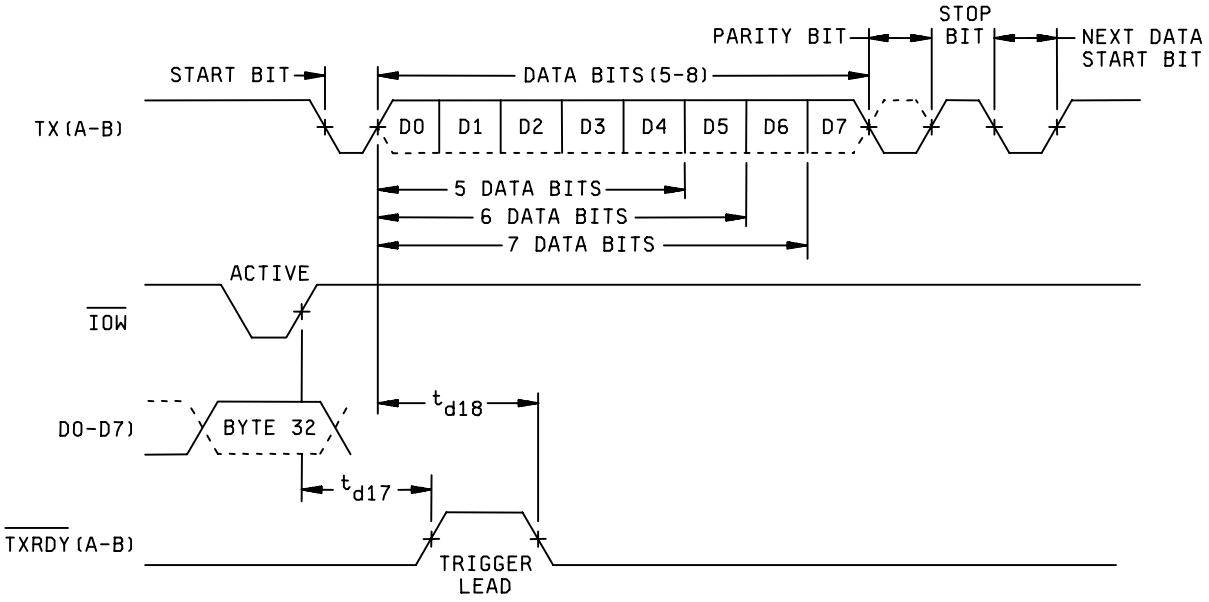


TRANSMIT TIMING



TRANSMIT READY TIMING IN NON-FIFO MODE

FIGURE 4. Timing waveforms – continued.



TRANSMIT READY TIMING IN FIFO MODE

FIGURE 4. Timing waveforms – continued.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6.0 NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/03626-01XE	01295	TL16C752BTPTREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493